COMPUTER ENGINEERING

A DEC VIEW OF HARDWARE SYSTEMS DESIGN

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790 machines had been shipped – more than the total of all other DEC 18-bit machines.

Two of the PDP-15 models are of special interest. A dual central processor version and the PDP-15/76. These are treated separately below.

DUAL CENTRAL PROCESSOR PDP-15

In 1973 the PDP-15 product line proposed and sold a system that was a dual processor. From the dual processor project came a dual port memory, which eventually was transferred to the PDP-15 standard product line. The dual port memory also expanded memory to the full 128 Kwords built into the PDP-15 addressing structure. The unit occupied a single rack and used the M-Series logic modules. Because there was space to add a third port within the rack unit, the dual port memory was actually built to be a three port device. At the time, the laboratory breadboard was an impressive array of three cabinets containing 128 Kwords of memory and two processors.

The logic included what went unrecognized as a "synchronizer" problem for two months, despite reviews by some senior engineers. The synchronizer problem, first described by Chaney and Molnar [1973] of Washington University, is a classical logic design problem that is theoretically unsolvable. When synchronizing (detecting) the presence of an event occurring at a random time relative to a fixed clock event, a small amount of energy is available to set the flip-flop. When the flip-flop is triggered with such a small signal, it can go into an undecided (metastable) state for a relatively long (even indeterminant) period of time. The problem occurred in the dual port memory design because the three inputs (2 ports and the memory clock) needed to be synchronized. Despite the theoretical lack of a solution, the practical solution is usually to wait longer (e.g., two clock times) or to improve the circuit by unbalancing it. Once the problem was recognized, the design went to a quick completion.

PDP-15/76

Of the systems listed in Table 2, the PDP-15/76 was one of the most interesting. A simplified block diagram of the final evolved state of the PDP-15/76 is shown in Figure 33. The diagram is referred to as an evolved design because the PDP-11 connection and the floating-point arithmetic features were not part of the original PDP-15 design.

The design of the PDP-15/76, also referred to as the Unichannel 15/76, began as a problem: find the most cost-effective way to attach a new moving head, removable platter disk to the PDP-15. After a review of the problem, it became clear that the correct way to solve the problem was to use a PDP-11 processor and the controller that had been designed for the PDP-11. The key reason for this was not the cost of designing a controller for the PDP-15, but rather the cost of writing a new set of disk diagnostics in PDP-15 code. (By that time, it was clear to all designers that hardware costs were swamped by software costs.)

As the system design progressed, it became clear that the PDP-11 could be used to run the other PDP-11 family peripherals that were the object of most of DEC's development and production efforts. The list of new peripherals quickly grew to include communications lines, plotters, printers, and card equipment. Figure 34 shows the options available for the PDP-15/76.

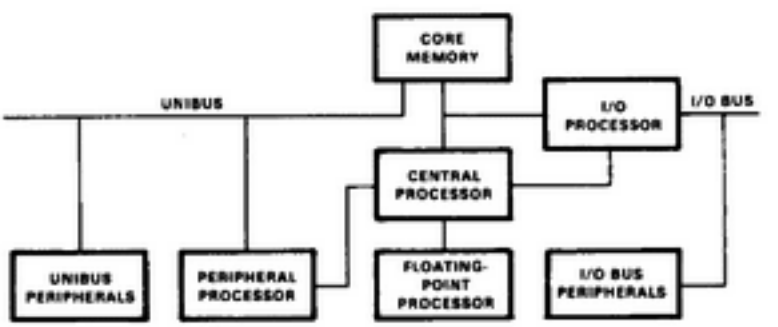

Figure 33. PDP-15/76 simple system block diagram.

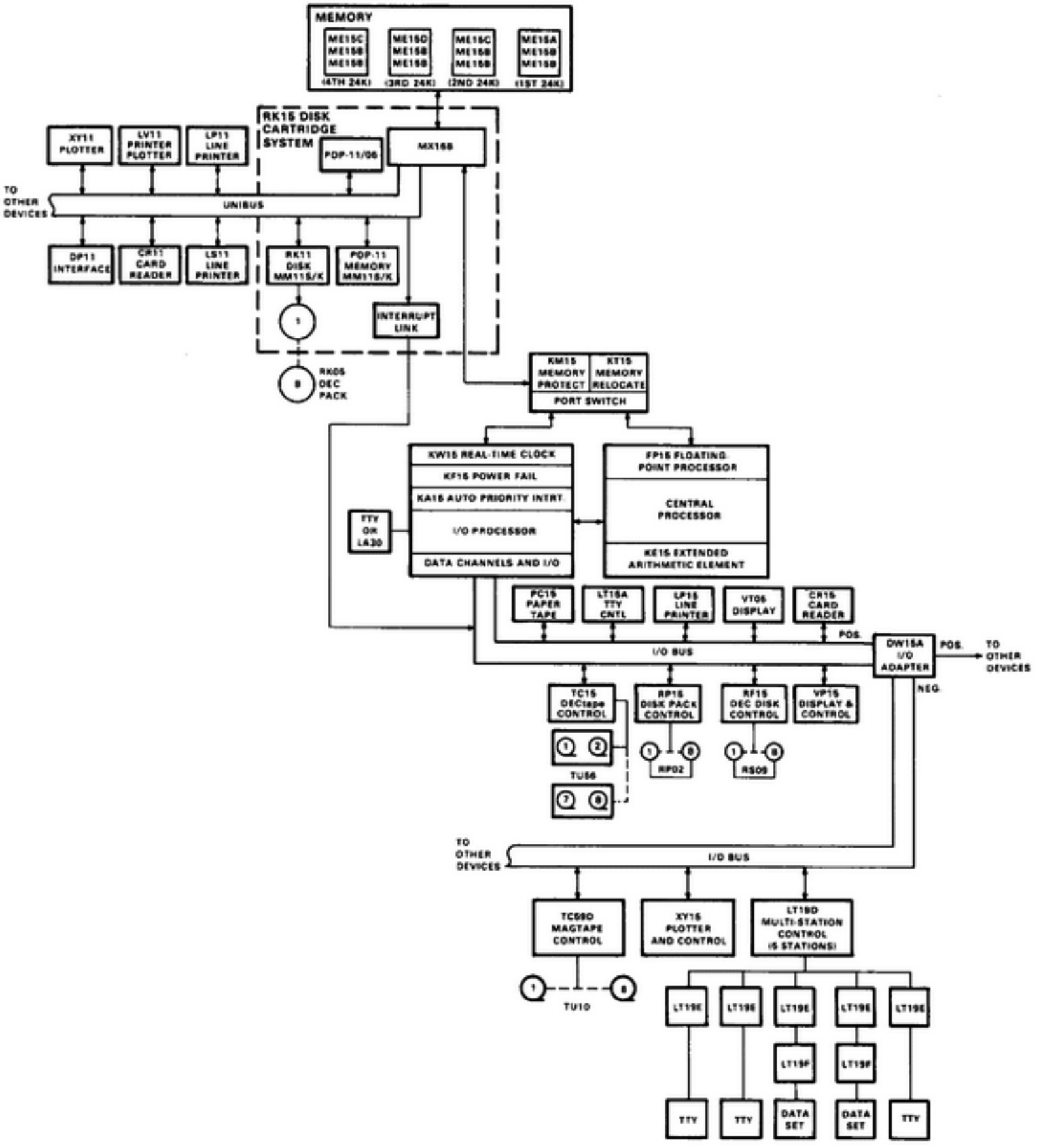

Figure 34. PDP-15/76 (XVM) system block diagram.

The project had a very small but excellent staff, and the hardware part of the program went very smoothly. Al Helenius did much of the logic design for the memory multiplexer device, using existing M-Series logic modules, and the prototype was operational in early November 1972. The complexity and size of the software task was clearly underestimated. However, the successful system operation depended on having more software. Rick Hully proposed an operating system structure that, for the era and application, was elegant, advanced, and yet straightforward. The reality was that the PDP-15/76 was a "multiprocessor" system, and today's terms "back-end processor" and "file processor" apply to what was accomplished on this machine in the early 1970s. Also, this structure was used by IBM in the coupled 7090/7044 system and the 360 Attached Support Processor.

From an application point of view, the PDP-15/76 dual processor system was extremely effective, especially in the following applications:

1. **Computer-aided design.** With the PDP-15 processor handling figures and computation while the PDP-11 processor handled an input digitizer, high speed plotter, and printer; with the PDP-11 and PDP-15 sharing memory and the new disk.
2. **Batch processing.** With the PDP-15 and the floating-point option handling computation while the PDP-11 handled spooling to printers, input from card readers, and terminals.

THE SERIES AND ITS EVOLUTION

It is useful to compare the five 18-bit computers that were designed over the course of roughly 10 years. The series began in the early second (transistor) generation and extended to the early part of the third (integrated circuit) generation. Had the series been extended to the fourth (large-scale integrated circuit) generation, a version of the PDP-15 could have been easily implemented on a single silicon chip. The paragraphs which follow each summarize the important characteristics of one or two members of the series, and Table 5 gives the technical information.

Contributions of Individual Machines to Series Development

The PDP-1 had a number of innovations over its laboratory predecessors, the Whirlwind and TX-0. It contributed extremely straightforward I/O interfacing capability together with a multichannel interrupt structure and Direct Memory Access capability which enabled a high I/O data rate. These characteristics made it ideal for high performance laboratory applications. The PDP-1 also represented a major stepping stone in the early days of timesharing computers. The message switching application contributed significantly to its market success and motivated the design of good communication interfaces in subsequent computers. Because the PDP-1 served as a thorough test vehicle for the circuitry of the 1000-series system modules, these modules were more suitable for their general application in building digital systems.

The PDP-4 contributed in small ways: there were minor improvements in the instruction set processor; and, because the PDP-4 was oriented to a much lower cost, some of the modules were refined. The simplified logic design of the PDP-4 was a major influence on the implementation style of subsequent computers. It also contributed the fundamental minicomputer notion that successor machines should be lower cost. Moreover, the PDP-4 extended the marketplace to industrial control, which had not been possible at PDP-1's price levels, and further improved the ease of I/O interfacing.

The PDP-7 and PDP-9 Families exploited a significant refinement in the wire-wrap packaging technology. Although the circuits were